Microperipheral MegaCore Library

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Family:
FLEX & MAX

Vendor:

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Features

- Library of standard functions: universal asynchronous receiver/transmitters (UARTs), programmable communications interface, direct-memory access (DMA) controller, and parallel port controller
- Optimized for the Altera® MAX® and FLEX® device architectures
- Fully verified and tested in MAX+PLUS® II and third-party environments
- Full design entry support in MAX+PLUS II as well as third-party tools, including tools from Cadence, Mentor Graphics, Synopsys, and Viewlogic
- Simulation models in VHDL and Verilog HDL, which support functional verification in third-party EDA tool environments
- MAX+PLUS II simulation vectors that demonstrate the functionality of each MegaCore™ function

General Description

The Microperipheral MegaCore Library includes several UARTs, a programmable communications interface, a DMA controller, and a parallel port controller. The Microperipheral MegaCore Library has been pre-tested, documented, and licensed by Altera as a MAX+PLUS II migration product. These functions are optimized for the architectural features of Altera devices, ensuring that user-specified performance and utilization goals are met. MegaCore functions reduce the design task to creating only the custom logic surrounding these commonly used system-level functions, dramatically shortening the design cycle. These functions permit designers to focus more time and energy on improving and differentiating the final product, rather than redesigning common off-the-shelf functions from the ground up.

Altera provides all files necessary to design with the Microperipheral MegaCore Library functions, including:

- A post-synthesis Altera Hardware Description Language (AHDL™) design file for design implementation in the target Altera device
- Test vectors for simulation in MAX+PLUS II
- VHDL and Verilog HDL functional simulation models for verification with standard EDA simulation tools

Functional Description

Table 1 describes each function and its logic cell requirements for MAX and FLEX devices.

Table 1. Logic Cell Requirements for Microperipheral MegaCore Functions *Note (1)*

MegaCore Function	Description	Logic Cell Requirements	
		MAX	FLEX
a8237	Programmable DMA controller	*Note (2)*	1,201
a8251	Programmable communications interface	*Note (2)*	528
a8255	Parallel port controller	128	194
a6402	UART	107	162
a16450	UART	307	372
a6850	Asynchronous communications interface adapter	330	237

Notes:
(1) The logic cell requirements are approximations.
(2) This function is too large for MAX devices.

Using the Microperipheral MegaCore Library Functions

Designers can use MAX+PLUS II or EDA tools to design and simulate these functions. For MAX+PLUS II design flows, the designer simply instantiates the function in the design file. For design flows that use third-party EDA tools, designers can instantiate a MegaCore function by specifying the function and port names in the hardware description language (HDL) design file. MAX+PLUS II compiles the resulting EDIF netlist file for the desired Altera device architecture.

The designer can use MAX+PLUS II to control compilation procedures. For example, designers can specify timing and performance requirements so that critical path requirements are met during place-and-route.

Vector Files (**.vec**) containing simulation vectors for these functions are provided in the **\megacore** directory on the MAX+PLUS II CD-ROM.

Evaluating MegaCore Functions Using the OpenCore Feature

Designers can preview Microperipheral MegaCore Library functions before purchase via the OpenCore™ feature. This pre-purchase evaluation system allows designers to instantiate and simulate MegaCore functions with the MAX+PLUS II software. However, programming files and output files for third-party EDA tool simulation can only be generated with an authorization code provided upon purchase of the library.

For further details on this library, refer to the ***Microperipheral MegaCore Library Data Book***.

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